REMARKS

This divisional application is being filed due to an election requirement contained in the Office Action dated 11/06/2003, in parent application serial no. 10/094,161.

Claims 114-128 are directed to a method for fabricating semiconductor components 16E (Figure 13F). As shown in Figure 13A, the method includes the step of providing a plurality of semiconductor dice 14E with die contacts 18E on a substrate 12E. As shown in Figure 13B, the method includes the step of forming contact bumps 24E on the die contacts 18E, and the step of forming an etch mask 84E on a back side of the substrate 12E. The etch mask 84E includes slots 86E in a criss cross pattern matching the peripheral outlines of the dice 14E. As shown in Figure 13C, the method also includes the step of forming a circuit side polymer layer 36E on the contact bumps 24E, which also has slots 88E in a criss cross pattern matching the peripheral outlines of the dice 14E. As shown in Figure 13D, the method also includes the step of planarizing the contact bumps 24E and the circuit side polymer layer 36E. As shown in Figure 13E, the method also includes the step of etching the substrate 12E from the circuit side 20E using the polymer layer 36E, and from the back side 22E using the etch mask 84E, to singulate the dice 14E. As shown in Figure 13F, the method also includes the step of removing the etch mask 84E, and forming a sealing layer 90E, such as parylene, on the singulated dice 14E.

Claims 129-141 are directed to a method for fabricating semiconductor components 16-1X (Figure 15F). As shown in Figure 15A, the method includes the step of providing a plurality of semiconductor dice 14-1X with die contacts 18-1X on a substrate 12-1X. As shown in Figure 15B, the method also includes the step of forming contact bumps 24-1X on the die contacts 18-1X. As shown in Figure

15C, the method also includes the step of forming a circuit side polymer layer 36P-1X, and planarizing the contact bumps 24-1X. As shown in Figure 15D, the method also includes the step of thinning the substrate 12-1X. As shown in Figure 15E, the method also includes the step of forming terminal contacts 42-1X on the contact bumps 24-1X, and a back side tape 100-1X on the substrate 12-1X. As shown in Figure 15F, the method also includes the step of singulating the dice 14T-1X from the substrate 12T-1X.

Claims 142-151 are directed to a method for fabricating semiconductor components 16D (Figure 17J). AS shown in Figure 17A, the method includes the step of providing a plurality of semiconductor dice 14D with die contacts 18D on a substrate 12D. As shown in Figure 17B, the method also includes the step of forming contact bumps 24D on the die contacts 18D, and trenches 28D in the substrate 12D. As shown in Figure 17C and 17D, the method also includes the step of forming polymer dams 108D in the trenches 28D. As shown in Figure 17F, the method also includes the step of forming a circuit side polymer layer 36DP using the polymer dams 108D, and then planarizing the circuit side polymer layer 36DP and the contact bumps 24D. As shown in Figure 17G, the method also includes the step of thinning the substrate 12DT from the back side. As shown in Figure 17H, the method also includes the step of forming terminal contacts 42D on the contact bumps 24D, and a back side polymer layer 38D on the substrate 12DT. As shown in Figure 17I, the method also includes the step of singulating the dice 14D from the substrate 12DT.

Also being submitted in the present application is an Information Disclosure Statement. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

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Stephen A. Gratton, Attorney for Applicants